

Application No.: 10/727220

Case No.: 59333US002

REMARKS

The Office Action dated May 12, 2005 has been received and reviewed. Claims 1, 12-15, 18, and 29 have been amended, and claim 28 has been cancelled. The pending claims are claims 1-27 and 29-39. Reconsideration and withdrawal of the pending rejections are respectfully requested.

Claim Amendments

Claim 1 has been amended to recite that each LED is electrically and thermally connected through the via to the electrically conductive layer.

Claims 12-15 have been amended to correct typographical errors.

Claim 18 has been amended to recite that the light emitting elements are electrically and thermally connected to the electrically conductive layer through the mounting vias.

Claim 29 has been amended such that it depends from claim 27.

No new matter has been added.

Allowable Subject Matter

Applicants acknowledge that claims 9, 19, and 23 were objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. However, Applicants submit that independent claims 1 and 18, from which the objected to claims depend, are in allowable form; therefore, Applicants have not amended claims 9, 19, and 23 at this time.

Further, Applicants acknowledge that claims 26-39 have been allowed.

The 35 U.S.C. § 102 Rejection

Claims 1, 3-8, 18-22, and 24 were rejected under 35 U.S.C. § 102(e) as being anticipated by Sugimoto et al. (U.S. Patent No. 6,874,910). Applicants note, however, that claim 19 was objected to; therefore, Applicants assume that claims 1, 3-8, 18, 20-22, and 24 are rejected under 35 U.S.C. § 102(e). Applicants traverse this rejection.

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However, to further move this case towards issuance, Applicants have amended claims 1 and 18. As amended, Applicants submit that claims 1, 3-8, 18, 20-22, and 24 are not anticipated by Sugimoto et al. because such reference does not teach each and every element of claims 1, 3-8, 18, 20-22, and 24.

For a claim to be anticipated under 35 U.S.C. § 102(e), each and every element of the claim must be found in a single prior art reference. See M.P.E.P. § 2131.

Claim 1 of the present application recites an illumination assembly that includes a substrate including an electrically insulative layer on a first side of the substrate and an electrically conductive layer on a second side of the substrate. The illumination assembly further includes a plurality of LED dies, where each LED die is disposed in a via extending through the electrically insulative layer on the first side of the substrate to the electrically conductive layer on the second side of the substrate. Claim 1 further recites that each LED die is electrically and thermally connected through the via to the electrically conductive layer on the second side of the substrate.

Further, claim 18 recites an illumination apparatus that includes a substrate having an electrically insulative layer on a first surface and an electrically conductive layer on a second surface, and a plurality of mounting vias extending through the electrically insulating layer to the electrically conductive layer. Claim 18 further recites a plurality of light emitting elements disposed in the plurality of mounting vias, where the light emitting elements are electrically and thermally connected to the electrically conductive layer through the mounting vias.

In contrast to claims 1 and 18, Sugimoto et al. describes a light source apparatus 1 that includes an LED chip 2 that is thermally coupled at one side to a radiator plate 3. See Sugimoto et al., column 10, lines 46-52. The radiator plate 3 is joined to an insulating member 4 with an adhesive 22. *Id.* at column 10, lines 53-56. The insulating member 4 has a through hole 6. *Id.* The LED chip 2 is die bonded to the radiator plate 3 in the opening formed by the through hole 6. *Id.* at column 11, lines 6-9. The apparatus 1 further includes a wiring pattern 8 that is provided on the upper side of the insulator member 4 where the radiator plate 3 is absent. *Id.* at column 11, lines 9-11. The two electrodes of the LED chip 2 are electrically connected to the wiring pattern 8 by bonding wires 9. *Id.* at column 11, lines 16-19.

The Office Action alleges that the insulating member 4 and the radiator plate 3 of Sugimoto et al. are equivalent to the substrate having an electrically insulative layer on a first side of the

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substrate and an electrically conductive layer on a second side of the substrate as recited, e.g., in claim 1 of the present application. The Office Action further alleges that Sugimoto et al. describes that the LED chip 2 is operatively connected through the through hole 6 to the radiator plate 3.

Applicants traverse this allegation. As can be seen in FIG. 1, Sugimoto et al. teaches that the LED chip is operatively connected to the wiring pattern 8, not the radiator plate 3. Further, claims 1 and 18 have been amended to recite that each LED is electrically and thermally connected through the via to the electrically conductive layer (claim 1), or that the light emitting elements are electrically and thermally connected to the electrically conductive layer through the mounting vias (claim 18). Sugimoto et al. does not teach that the LED chip 2 is electrically and thermally connected to the radiator plate 3. Because Sugimoto et al. does not teach each and every element of claims 1 and 18 as alleged by the Examiner, such claims are not anticipated by Sugimoto et al.

Claims 3-8, 20-22, and 24, which depend either from independent claim 1 or claim 18, are not anticipated by Sugimoto et al. for the same reasons as presented above for claims 1 and 18. In addition, claims 3-8, 20-22, and 24 each recite additional elements that further support patentability when combined with either claim 1 or claim 18.

Further, Applicants traverse the Office Action's allegation that claims 4-6 recite product by process limitations. For example, claim 4 recites that the via extending through the electrically insulative material is chemically etched, claim 5 recites that the via is plasma etched, and claim 6 recites that the via is laser milled. Applicants submit that a chemically etched via may have different structural properties than a plasma etched or laser milled via. For example, chemically etched vias may have sloped side walls (e.g., sloped side walls 49 of FIG. 3A of the present application); however, vias that are plasma etched or laser milled may have substantially vertical side walls (e.g., vertical side walls 49 of FIG. 3A). See, e.g., Specification, page 3, ¶ 0040 (of the Patent Publication).

For at least the above reasons, Applicants submit that claims 1, 3-8, 18, 20-22, and 24 are patentable over Sugimoto et al. Therefore, reconsideration and withdrawal of the rejections are respectfully requested.

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The 35 U.S.C. § 103(a) Rejection

Claims 2 and 25 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Sugimoto et al. in view of Matsui et al. (U.S. Patent Publication No. 2003/0052594 A1).

Applicants traverse this rejection.

However, to further move this case towards issuance, Applicants have amended claims 1 and 18, from which claims 2 and 25 depend. Applicants submit that claims 2 and 25 are not *prima facie* obvious because the combination of Sugimoto et al. and Matsui et al. does not teach all of the elements of claims 2 and 25.

To establish a *prima facie* case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art references must teach or suggest all the claim limitations. See M.P.E.P. § 2143.

As described above in regard to the 35 U.S.C. § 102(e) rejection of claims 1 and 18, Sugimoto et al. does not teach all of the elements of claims 1 and 18, e.g., Sugimoto et al. does not teach that the LED chip 2 is electrically and thermally connected to the radiator plate 3. In addition, claims 2 and 25, which depend from either independent claim 1 or claim 18, recite additional elements that further support patentability when combined with either claim 1 or claim 18. The addition of Matsui et al. does nothing to cure this deficiency already present in Sugimoto et al.

For at least the above reasons, Applicants submit that claims 2 and 25 are patentable over the cited references. Reconsideration and withdrawal of this rejection are, therefore, respectfully requested.

Claims 10-17 were also rejected under 35 U.S.C. § 103(a) as being unpatentable over Sugimoto et al. Applicants traverse this rejection and submit that claims 10-17 are not *prima facie* obvious in view of Sugimoto et al. because such reference does not teach all of the elements of claims 10-17.

Claims 10-17 depend from independent claim 1. As described above in regard to the 35 U.S.C. § 102(e) rejection of claim 1, Sugimoto et al. does not teach all of the elements of claim

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1. Further, claims 10-17 recite additional elements that further support patentability when combined with claim 1.

For at least the above reasons, Applicants submit that claims 10-17 are patentable over Sugimoto et al. Reconsideration and withdrawal of the rejection are, therefore, respectfully requested.

Summary

It is respectfully submitted that the pending claims are in condition for allowance. Reconsideration and withdrawal of all rejections are respectfully requested. The Examiner is invited to contact Applicants' Representatives, at the below-listed telephone number, if it is believed that prosecution of this application may be assisted thereby.

Respectfully submitted,

August 11, 2005
Date

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